

## REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of October 10, 2007 is respectfully requested.

In the outstanding Office Action, the Examiner rejected pending claims 1-8 as being anticipated by the Basol reference (USP 6,943,112); rejected claim 9 as being unpatentable over the Basol reference in view of the Nagai reference (US 2002/0027081); and rejected claim 27 as being unpatentable over the Basol reference in view of the newly-cited Arya reference (USP 4,749,454). However, independent claim 1 has now been amended so as to clarify the process of applying a reverse electric field, and dependent claim 27 has therefore been cancelled. For the reasons discussed below, it is respectfully submitted that amended independent claim 1 and the claims that depend therefrom are clearly patentable over the prior art of record.

As generally discussed on pages 1-4 of the original specification, conventional plating methods often encounter difficulties due to voids being created during the plating process, particularly when the plating process is performed on a substrate that has both narrow recesses and relatively broad recesses in the surface to be plated. The present invention has been developed in order to provide a plating method which overcomes the problems involved in the conventional plating methods, and thereby provide a void-free plated metal film on the substrate (see page 5, lines 9-15 of the original specification).

In particular, the invention recited in amended independent claim 1 is directed to a plating method that comprises performing *first plating* for filling a metal in a narrow recess of a substrate, and performing *second plating* for filling a metal in a broad recess in the substrate. After the plated film is formed by the first plating process, and before the second plating process is performed, a reverse electric field is applied *for a period of time in a range of 1 second to 4 seconds* so as to etch the plated film filled in the narrow recess (see page 8, line 28 through page 9, line 6 of the original specification).

As explained on page 9 of the original specification, the reverse electric field is applied after the first plating in order to etch away any overplated film on the surface of the narrow recesses. As a result, any additive that is specific to the particular plating conditions for the first

plating can be removed with the overplated film so as to prevent that additive from interfering with the second plating. Simultaneously, the surface of the plated film is quickly and efficiently prepared for the second plating (see also page 21, line 24 through page 22, line 3 of the original specification). By limiting the time period during which the reverse electric field is applied to within a range of 1 second to 4 seconds, the overplated film is sufficiently removed, but the desirable plated film within the narrow recesses will remain.

In the outstanding Office Action, the Examiner asserted that the Basol reference teaches reversing the applied voltage, and referred to column 9, lines 35-52 of that reference. However, the Basol reference simply teaches that the applied voltage is reversed, but does not even vaguely specify the length of time during which a reverse electric field should be applied. At the bottom of page 5 of the Office Action, the Examiner agreed that the Basol reference does not disclose application of a reverse electric field for a period between 1 to 10 seconds. In fact, as noted above, the Basol reference does not teach or even suggest any particular length of time for the application of a reverse electric field.

Nonetheless, the Examiner asserted that the newly-cited Arya reference teaches a semiconductor processing method in which a reverse-bias voltage is applied from 5 to 7 seconds (column 5, lines 13-31). However, independent claim 1 has now been amended as indicated above to clarify that the reverse electric field is applied for a period of time *in a range of 1 second to 4 seconds*, which is clearly outside of the specified range in the Arya reference. Consequently, it is submitted that the Arya reference does not teach or even suggest the time range for applying the reverse electric field as now set forth in amended independent claim 1.

Moreover, it is submitted that one of ordinary skill in the art would not be motivated to utilize the time range for application of the reverse-bias voltage as set forth in the Arya reference to modify the Basol reference as suggested by the Examiner. Specifically, the Arya reference concerns a method of removing electric shorts and shunts from a semiconductor device. In other words, the Arya reference does not relate to a *plating method*, but rather relates to a method of improving an existing semiconductor device. Because the Arya reference does not even relate to

a plating method, it is submitted that one of ordinary skill in the art would not look to the teachings of the Arya reference to modify the plating process taught in the Basol reference.

As explained above, the Arya reference (as well as the other prior art references of record) does not teach or suggest applying a reverse electric field for a period of time in a range of one second to four seconds between a first plating process and a second plating process. In fact, the Arya reference does not even relate to a plating process. Therefore, because the Basol reference also does not teach this feature, there is no apparent reason for one of ordinary skill in the art to obtain the plating method as recited in amended independent claim 1. Accordingly, it is respectfully submitted that amended independent claim 1 and the claims that depend therefrom are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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